EXPRESS MAIL NO EV530945820US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Rakesh Malik et al.
Application No.	:	09/807,500
Filed	:	June 11, 2001
For	:	AREA EFFICIENT REALIZATION OF COEFFICIENT ARCHITECTURE FOR BIT-SERIAL FIR, IIR FILTERS AND COMBINATIONAL/SEQUENTIAL LOGIC STRUCTURE WITH ZERO LATENCY CLOCK OUTPUT

Examiner	:	Chat C. Do
Art Unit	:	2193
Date of Notice of Allowance	:	May 3, 2005
Docket No.	:	851663.422USPC
Date	:	August 2, 2005

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER ALLOWANCE

(UNDER 37 CFR 1.312)

Commissioner for Patents:

In response to the Notice of Allowance dated May 3, 2005, please amend the application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Drawings begin on page 4 of this paper and include an attached Replacement Sheet.

Remarks/Arguments begin on page 5 of this paper.